WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a semiconductor substrate having source/drain regions spaced from each other;

a gate pattern disposed on the semiconductor substrate between the source/drain regions, said gate pattern having opposite side walls;

L-shaped spacers each including a vertical portion covering a respective one of the side walls of the gate pattern, and a lateral portion extending laterally from the bottom of the vertical portion over a respective one of the source/drain regions; and

support portions interposed between said L-shaped spacers and the gate pattern, said support portions supporting said L-shaped spacers such that the lateral portion of each of the L-shaped spacers is spaced above the source/drain region over which the lateral portion of the L-shaped spacer extends, and wherein an air gap exists between the lateral portion of each of the L-shaped spacers and the source/drain region over which the lateral portion extends.

2. The semiconductor device according to claim 1, wherein the source/drain region comprises a lightly-doped source/drain region over which the lateral portion of one of said L-shaped spacers extends, and a highly-doped source/drain region disposed laterally of the lateral portion of the L-shaped spacer.

3. The semiconductor device according to claim 1, wherein said L-shaped spacers comprise an oxide layer.

4. The semiconductor device according to claim 1, wherein said support portions comprise a polysilicon layer or a nitride layer.

5. The semiconductor device according to claim 1, and further comprising a buffer insulating layer interposed between said gate pattern and said support portion.

6. A method of fabricating a semiconductor device, comprising:

forming a gate pattern on a semiconductor substrate, wherein the gate pattern has opposite side walls;

forming a support layer, a spacer insulating layer and a sacrificial layer sequentially on the semiconductor substrate including over the gate pattern;

anisotropically etching the sacrificial layer, the spacer insulating layer, and the support layer so as to form L-shaped support patterns covering the side walls of the gate pattern and respective portions of the semiconductor substrate adjacent to the gate pattern, L-shaped spacers covering the L-shaped support patterns, and sacrificial patterns covering the L-shaped spacers, wherein the L-shaped spacers each include a vertical portion normal to the semiconductor substrate and a lateral portion extending laterally from the bottom of the vertical portion;

isotropically etching the L-shaped support patterns from between at

least the lateral portions of the L-shaped spacers and the semiconductor substrate so as to form an air gap between the lateral portions of the L-shaped spacers and the semiconductor substrate; and

implanting ions into the semiconductor substrate, including using the gate pattern and the L-shaped spacers as an ion implantation mask, so as to form source/drain regions in the semiconductor substrate adjacent the gate pattern.

7. The method of fabricating a semiconductor device according to claim 6, wherein the support layer and the sacrificial layer are formed of the same material.

8. The method of fabricating a semiconductor device according to claim 7, wherein the sacrificial pattern is removed during the etching of the L-shaped support pattern.

9. The method of fabricating a semiconductor device according to claim 6, wherein said forming of the spacer insulating layer comprises forming an oxide layer on the support layer.

10. The method of fabricating a semiconductor device according to claim 9, wherein said forming of the support layer comprises forming a polysilicon layer or a nitride layer on the semiconductor substrate.

11. The method of fabricating a semiconductor device according to claim 9, wherein said forming of the support layer comprises forming a semi-insulating polysilicon layer on the semiconductor substrate.

12. The method of fabricating a semiconductor device according to claim 9, wherein said forming of the sacrificial layer comprises forming a polysilicon layer or a nitride layer on the spacer insulating layer.

13. The method of fabricating a semiconductor device according to claim 6, wherein said implanting of ions into the substrate comprises forming a respective lightly-doped source/drain region beneath the lateral portion of each of the L-shaped spacers and forming a highly-doped source/drain region contiguous to the lightly-doped source/drain region.

14. The method of fabricating a semiconductor device according to claim 6, and further comprising forming a buffer insulating layer between the gate pattern and the support layer.

15. A method of fabricating a semiconductor device, comprising:

forming a gate pattern on a semiconductor substrate, wherein the gate pattern has opposite side walls;

forming a buffer insulating layer on the semiconductor substrate including over the gate pattern, the buffer insulating layer being of a material having an etch selectivity with respect to the gate pattern;

forming a support layer, a spacer insulating layer and a sacrificial layer sequentially on the semiconductor substrate including over the gate pattern, wherein the support layer and the sacrificial layer are of the same material and have an etch selectivity with respect to the spacer insulating layer;

anisotropically etching the sacrificial layer, the spacer insulating layer, and the support layer so as to form L-shaped support patterns covering the side walls of the gate pattern and respective portions of the semiconductor substrate adjacent to the gate pattern, L-shaped spacers covering the L-shaped support patterns, and sacrificial patterns covering the L-shaped spacers, wherein the L-shaped spacers each include a vertical portion normal to the semiconductor substrate and a lateral portion extending laterally from the bottom of the vertical portion;

removing the sacrificial patterns, and isotropically etching the L-shaped support patterns so as to provide an air gap between at least the lateral portion of each of the L-shaped spacers and the semiconductor substrate; and

implanting ions into the semiconductor substrate, including using the gate pattern and the L-shaped spacers as an ion implantation mask, so as to form source/drain regions in the semiconductor substrate adjacent the gate pattern.

16. The method of fabricating a semiconductor device according to claim 15, wherein said forming of the gate pattern comprises forming a gate electrode of polysilicon.

17. The method of fabricating a semiconductor device according to claim 16, wherein said forming of the buffer insulating layer comprises forming an oxide layer on the semiconductor substrate including over the gate pattern.

18. The method of fabricating a semiconductor device according to claim 15, wherein said forming of the spacer insulating layer comprises forming an oxide layer on the support layer.

19. The method of fabricating a semiconductor device according to claim 18, wherein said forming of the support layer and the sacrificial layer each comprise the forming of a polysilicon layer or a nitride layer.

20. The method of fabricating a semiconductor device according to claim 15, wherein said implanting of ions into the substrate comprises forming a respective lightly-doped source/drain region beneath the lateral portion of each of the L-shaped spacers and forming a highly-doped source/drain region contiguous to the lightly-doped source/drain region.